



RESUME

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EDUCATION

1980-1983 University of Massachusetts, Amherst, U. S. A.

Ph.D. (Electrical and Computer Engineering)

Dissertation : "Monte Carlo simulation of MOSFET and Bipolar Transistors"

1975-1977 Seoul National University, Seoul, Korea

M.S. (Electrical Engineering)
Thesis : "MOS Capacitor Fabrication and Study on the Si-SiO₂ Interface"
1971-1975 Seoul National University, Seoul, Korea
B.S. (Electrical Engineering)

EXPERIENCE

1997 - Professor, School of Electrical Engineering, Seoul National University, Has advised 27 Ph.D. Students, 31 Master students.

2003 - Director of "Nano Systems Institute_ National Core Research Center" of the Seoul National University

2001-2002 Director, Hynix semiconductor, memory R&D

2000-2002 Director of the Inter-university Semiconductor Research Center of the Seoul National University

1999-2001 Director of "A Collaborative Project for Excellence in Basic System IC Technology"

1996-1998 Director of "National Project on Next Generation Semiconductor Technology"

1995-1997 Director of the Inter-university Semiconductor Research Center of the Seoul National University

1992-1997 Associate Professor, School of Electrical Engineering, Seoul National University

1988-1992 Assistant Professor, Dept. of Electronics Engineering, Seoul National University

1992-1993 Visiting Scholar, Integrated Circuit Laboratory, Stanford University

1985-1988 Principal Scientist, Gold Star Semiconductor R&D, Korea
Developed high performance CMOS and BiCMOS Technology

1983-1985 Researcher, IBM, East Fishkill, New York
Developed Advanced Modeling for Bipolar Technology used for Next generation IBM main computer

1977-1980 Instructor, Korea Naval Academy, Jinhae, Korea
Taught Physical Electronics, Circuit Theory and Logic Design
Developed Finite Element Analysis Program of Bipolar Transistor

Awards/Honors/Professional Accomplishments

1. The award of republic of Korea naval academy (1979)
2. The award of the president of LG cooperation for developing 4MD DRAM(1986)
3. The best teacher award : Seoul National University (1999)
4. Tin Tower Order of Industrial Service Merit: President of Korea (2002)
5. Member of NAEK (National Academy of Engineers of Korea)(from 2004)

Contributions to Industry

-Director of Memory R&D of Hynix Semiconductor, Inc.,(2000-2002) on leave of absence from Seoul National University.

As the Director of R&D with more than 2000 engineers under his advice, he led the 'blue chip' project for 256MDRAM family to make the DRAM process most efficient and suitable to the I

line steppers (rather than scanners) based process. The efforts turn the company, which once was under the law of reconstruction initiated by the banks, to most profitable semiconductor company in the world.

As the consequence of the efforts, he was awarded the 'Industrial Service Merit' from the president of Korea, Kim DaeJoong in 2002. After leaving he served as the consultant to the company in the area of reliability enhancement of the DRAM and Flash memory from 2002-2005.

Achievements in R&D

– Advanced Carrier transport modeling

Hybrid method to mix the 'Monte Carlo method' and "drift diffusion model" in the silicon device. Monte Carlo method was proposed in 1983 []. In the hybrid model, the Monte Carlo method is applied to the region where non static transport is important and the drift diffusion model is applied to the regions where the static transport approximation model is valid. The coupling of two methods have been performed by feed back the information of total velocity of carriers from Monte Carlo region in the form of Quasi Fermi level to the drift diffusion model. The method was first applied to the advance bipolar transistor to predict the right f_T value. The method has been subsequently used by the Stanford group under the name of "Windowed Monte Carlo method" for the modeling of advanced MOSFET devices.

– TEHD (Tail Electron Hydrodynamic model): Developed the Hybrid method where the transport of the hot carriers having energy higher than a certain energy level of interest (1.1eV for impact ionization and 3eV for hot carrier injection toward SiO₂ as an example) is treated as a separate group of electrons, called the tail electrons. The continuity equations for the group of electrons are set up and solved independently from the rest. The work was performed with the Prof Dutton's group of Stanford university in 1994.

The work resulted in the series of papers in IEEE.

– Device and circuit technology

Developed the series of circuits with bulk of the MOSFET devices are controlled by gates. Especially the techniques are applied to the Charge pumping circuits to remove the voltage loss due to the back bias effects during the charge transfer to the subsequent stage. The techniques are published in IEEE, J. of Solid State Circuits and filed to Korea patent # 10-0296861-0000.

The technique is used as the standard charge pumping circuits used for most advanced NAND Flash memory more than 70% used in the world.

Contributions to Academic society

- IEEE IEDM; served as the subcommittee member of "CMOS technology" from 2001-2003
- KITE president of Semiconductor Sector
- Director of Korean national semiconductor project(system 2010 project) from 1999-2001